NANO LETTERS

2007
Vol. 7, No. 12
3840−3844

Graphene Transistors Fabricated via Transfer-Printing In Device Active-Areas on Large Wafer

Xiaogan Liang, Zengli Fu, and Stephen Y. Chou*

NanoStructure Laboratory, Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08544

Received October 5, 2007; Revised Manuscript Received November 3, 2007

ABSTRACT

We demonstrate a method that uses the pillars on a stamp to cut and exfoliate graphene islands from a graphite and then uses transfer printing to place the islands from the stamp into the device active-areas on a substrate with a placement accuracy potentially in nanometers. The process can be repeated to cover all device active-areas over an entire wafer. We also report the transistors fabricated from the printed graphene. The transistors show a hole and electron mobility of 3735 and 795 cm^2/V-s, respectively, and a maximum drive-current of 1.7 mA/μm (at $V_{DS} = 1$ V), which are among the highest reported for room temperature. The effects of various transferring and fixing layers on sticking graphenes to a stamp and to a substrate, respectively, were also investigated.

Graphene is of great interest as a material for making future transistors because of its high mobility, high saturation velocity for both electrons and holes, stable crystal structure, and ultrathin layer thickness. The electrical transport advantages have been clearly demonstrated by the transistors fabricated using exfoliation[1−4] or epitaxial growth.[5] However, to use graphene as the material for integrated circuits we need high-quality graphene on large, preferably 8 in. or bigger, wafers. One major challenge today is that we can produce only small pieces (approximately tenths of a micrometer) of single-domain graphene and not over entire 8 or 12 in. wafers.

This paper reports a demonstration of a different approach to achieve high-quality graphene on large substrates suited for the fabrication of integrated circuits, and a demonstration of the transistors fabricated on printed graphene. The method, termed graphene-on-demand by cut-and-choose transfer-printing (DCT), does not intend to put high-quality graphene everywhere on a large substrate but rather only in each device active-area of such substrate, which is often a size of tenths of micrometers. As shown in Figure 1, DCT uses pillars (protrusions) of a stamp to cut and exfoliate a high-quality graphene piece (one piece per pillar) from a graphite then inspects them. If an inspected graphene is good, it will be printed on the device active-area of a wafer with high-placement precision (using the alignment marks on the wafer and the stamp). The cut-choose and print process will be repeated to have graphenes on all device active areas of an entire wafer. The alignment marks on the wafer allow precise placements of not only the graphenes on a wafer but also other device structures on the graphene to complete a device.

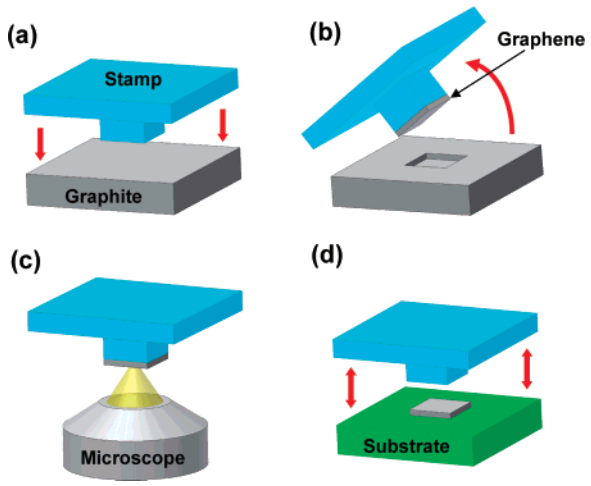

Figure 1. Schematic of graphene-on-demand by cut-and-choose transfer-printing (DCT). (a) Press the stamp with protrusions into the graphite substrate; (b) the stamp cuts and attaches a piece of graphene using its protrusion edge, and then the separation of the stamp from the graphite exfoliates the cut graphene sheet; (c) inspect the quality of the graphene sheet that is attached on the stamp protrusion; and (d) if the graphene is good, transfer the graphene sheet onto the device active-area of another substrate.

The current demonstration is on the cutting, exfoliating, and printing and not yet on choosing. The DCT stamps in our experiments have pillars of various patterns including 1.8−20 μm diameter pillar arrays and were made out of silicon with a thin oxide. The pillars were fabricated using

* Corresponding author. E-mail: chou@princeton.edu.

10.1021/nl072566s CCC: $37.00
Published on Web 11/14/2007

photolithography followed with inductively coupled plasma etching. Hence, the alignment marks can be fabricated at the same time. The mold fabrications are silimar to that for nanoimprint molds.[6,7] The graphite material was obtained from Structure Probe, Inc. (Grade SPI-1) and is a highly orientated pyrolytic graphite.

Before cutting and exfoliating a graphene, the top of the pillars on the stamp was coated with a thin "transferring" layer (T-layer), whose function is to "glue" graphene layers to the stamp during cutting and exfoliating, but can release under certain conditions the bonding between the graphene and the stamp once the graphene is printed on a wafer. There are many ways to create the transferring layer. One of the T-layers that we developed is a resin-based material that can be spin-coated on the stamp surface with a ~10 nm thickness and behaves like a glue at room temperature without any further treatment. However, as discussed later we found that the "release the bonding" from a transfer media might not be necessary for a transfer-printing.

Graphene layers were cut from a graphite by pressing the stamp coated with a T-layer into the graphite at a pressure of 300 psi and room temperature for 4 min, using an nanoimprintor (e.g., Nanonex-2000, which has air cushion press for pressure uniformity).[8] The shear force created by high-stress gradient at the stamp pillar edges causes fractures and hence cuts the graphenes along the pillar edges. Previously, it had been observed that the edges of the structured stamp can cut off patterns in organic thin films.[9,10]

After cutting the graphene, the stamp was separated from the graphite by using a homemade separator at room temperature. Because the T-layer is a good room-temperature glue and bonded the stamp to the graphite surface well, the separation exfoliated a thin layer of graphenes from the graphite bulk.

Before printing the exfoliated graphene on a substrate, the substrate surface was coated with a "fixing" layer (F-layer) to provide a good adhesion between the substrate and the graphene during the printing using the stamp. Clearly, the F-layer should have a bonding between the substrate and the graphene stronger than either between the stamp and the graphene or between the graphene layers. During the transfer printing, the stamp was pressed on a substrate at room temperature or an elevated temperature for a certain time and then was separated from the substrate. The elevated temperature can be used to increase the bonding between the graphene and substrate, and/or release the T-layer. The conditions for printing graphenes on the SiO_2 surface are different from that for printing organic film and metal,[11,12] because the graphene itself has a very weak surface bonding.

We have developed and used several fixing layers. One of the F-layers is a thermal curable glue with extremely low viscosity, which results in ~10 nm thickness after the printing of the graphene on it. After curing, the material becomes solid and a good dielectric. The other F-layer is simply the dangling bonds created on the substrate surface by using an oxygen plasma, which is known to create a bonding surface.[13,14] Furthermore, we found that even pressing an exfoliated graphene on a stamp directly on a clean SiO_2 surface can create a rather good bonding. We found that all these three wafer−graphene-bonding methods can have a bonding strength, so that a separation of the stamp and the substrate would further split the thin graphene layer into two, one on the substrate and the other on the stamp. An advantage of the fixing layer using either an oxygen plasma-treated surface or a clean plasma-untreated surface is that the fixing layer has nearly zero thickness, and hence is well suited for making field-effect transistors (FETs).

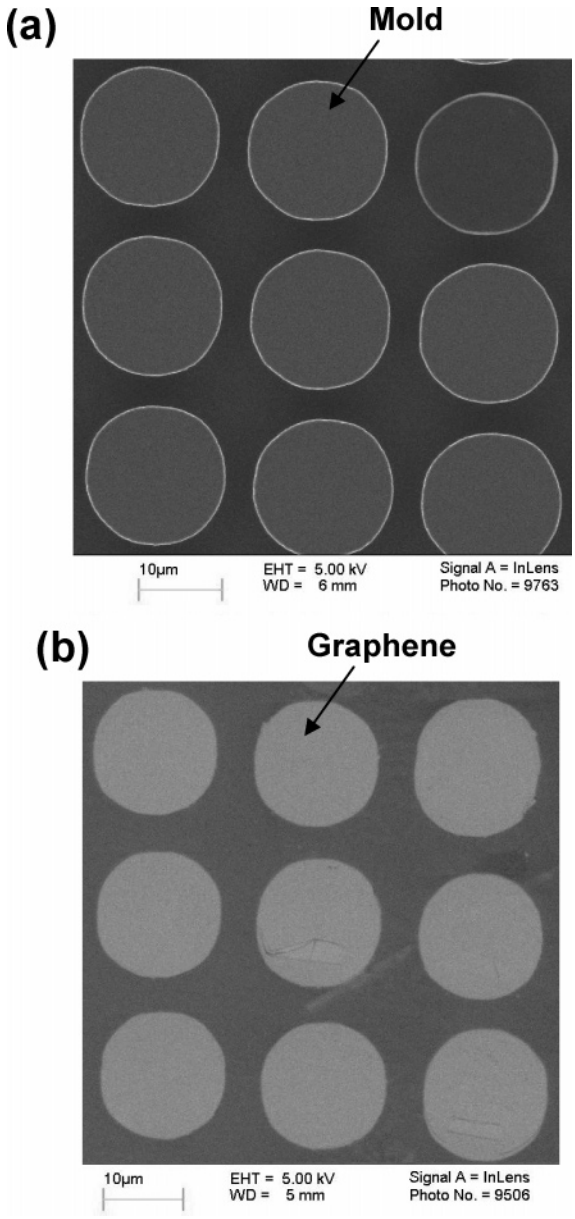

Figure 2. SEM images of (a) a DCT stamp of 15 μm diameter pillar array, and (b) the graphene flake array that was cut from a graphite and transfer-printed on a SiO_2 surface of another substrate using the DCT stamp in panel a.

Figure 2 shows the scanning electron microscopy (SEM) images of the stamp and the graphene transfer printed on SiO_2/Si substrate. The stamp was made of Si with a thin SiO_2 layer and has pillars of 15 μm diameter (50 μm tall). The cutting of graphene was performed by pressing the pillars on the stamp (Figure 2a). The graphene cut has the same shapes (Figure 2b) as the pillars on the stamp, indicating

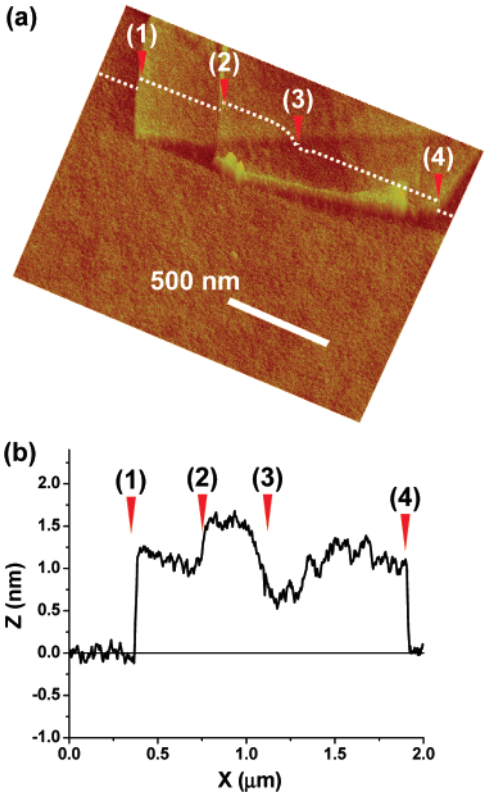

Figure 3. An AFM image of a graphene flake that was cut from a graphite bulk and transfer-printed on a SiO_2/Si substrate using a 1.8 μm diameter pillar on a stamp. (a) Tilted view and (b) a line scan. The points (1) and (4) are the boundaries between the graphene and the substrate, and the points (2) and (3) are the thickness variation within the graphene sheet. The average thickness is 1.2 nm (4 graphene layers) and the variation is about 0.6 nm (2 graphene layers).

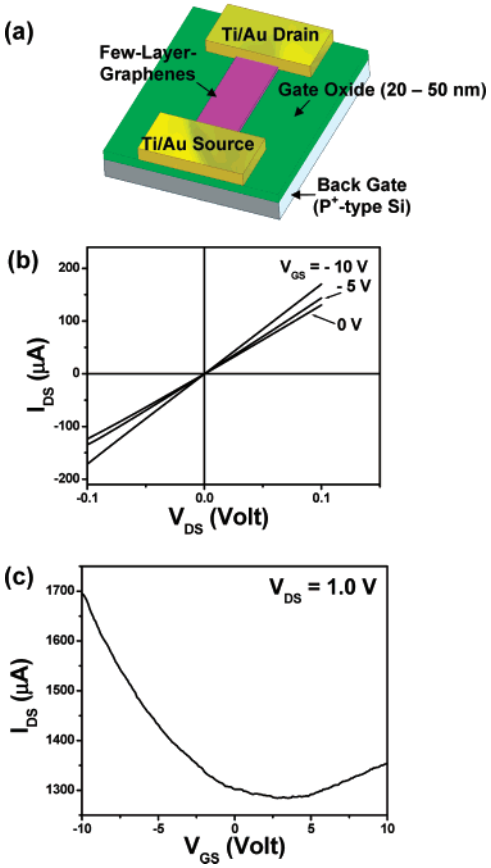

Figure 4. (a) Schematic of the back-gated graphene field-effect transistor (FET) with the SiO_2/Si substrate serving as the gate dielectric and the back gate. (b) Drain-source current (I_{DS}) vs the drain-source voltage (V_{DS}) under different gate voltages ($V_{GS} = 0$, 5, 10 V). (c) I_{DS} vs V_{GS} for a fixed $V_{DS} = 1$ V, $V_{GS} = -10$ to 10 V (back gate field E_{BG} from -5 to 5 MV/cm); the drain-source current I_{DS} exhibits an ambipolar behavior, both electron and hole conductions, and the current minimum occurs at $V_{GS} \sim 3.1$ V. The average transconductance per width at $V_{DS} = 1$ V was extracted to be $g/W = (\partial I_{DS}/\partial V_{GS})/W = 53.3$ μS/μm

that most of the cut was caused by high-shear stress-induced fractures at the stamp edges and not by tearing. The fixing layer for graphene shown in Figure 2b is not a curable polymer layer but an oxygen treated SiO_2 surface on the substrate. During the printing, the transferring layer is not released but bonds to one side of the cut-and-exfoliated graphene, and hence the separation between the stamp and the substrate further exfoliates the original graphene on the stamp into two thinner pieces: one is on the stamp, and the other is on the substrate.

The graphene can be printed precisely into device active-areas of a substrate, because both the substrate and the stamps can have prefabricated alignment marks and can be used during a transfer printing. Previously, it has shown that when Morie pattern-based alignment marks are used, the alignment accuracy can be far better than 20 nm.[15]

We used atomic force microscopy (AFM) to measure the thickness of the graphene flakes transfer printed onto SiO_2/Si substrates with the oxygen plasma-treated surface as the fixing layer (hence nearly zero F-layer thickness). The AFM image of a printed graphene sheet (Figure 3) shows that the average thickness of the sheet is ~1.3 nm, namely about 4 graphene monolayers (the interlayer spacing of graphenes is ~ 0.34 nm[1]), and there is a thickness variation of between 1 to 1.5 nm in the sheet. Further AFM imaging of other printed graphenes over the whole wafer shows a typical thickness in the range from 0.9 (~3 monolayers) to 5 nm (~15 monolayers) with a fluctuation of graphene thickness of 1.2 nm (~4 monolayers).

We have fabricated FETs on the graphene printed on a SiO_2 surface (20−50 nm thick) thermally grown on a Si substrate (Figure 4a). The substrate, p + Si (resistivity ~0.2 Ω cm), serves as a back-gate for the FET (Figure 4a). The graphene flakes with a thickness of 1.2 (~4 monolayers) to 3 nm (~9 monolayers) were chosen because they are the thinnest films but are still visible and can be located for patterning the contact pads using a Karl Suss MA6 photo-aligner. Using photolithography, electron-beam evaporation, and metal lift-off, 10 nm Ti/100 nm Au source and drain pads were formed. A metal contact was made to the substrate as the back-gate contact. The back-gated graphene FETs were characterized by using an HP-4145B semiconductor parameter analyzer (Hewlett-Packard).

The transistors were fabricated on the fixing layers using a bonding with either plasma-untreated or plasma-treated oxide surfaces. For the bonding with plasma-untreated oxide

surface, the $I-V$ characteristics of a FET with the graphene thickness of $d \sim 1.5$ nm, a gate oxide thickness of $t_{ox} = 20$ nm, the graphene channel width of $W = 1$ μm, and the channel length of $L = 10$ μm are shown in Figure 4b,c. The linear I_{DS} versus V_{DS} behavior (Figure 4b) indicates a good ohmic contact between Ti/Au contact pads and graphene channels. The I_{DS} versus V_{GS} curve (Figure 4c) shows that the gate can cause either hole or electron conduction. The transition point is at $V_{GS} \sim 3.1$ V.

For the measured $I-V$ characteristics in linear region, the carrier (hole and electron) mobilities can be deduced by using eq 1, where μ is the carrier mobility, W and L are FET width and length, respectively, $C_{ox} = \epsilon_{ox}\epsilon_0/t_{ox}$ is the gate oxide capacitance ($\epsilon_{ox} = 3.9$ is silicon dioxide permittivity and t_{ox} is the gate oxide thickness), and ΔI_{DS} is induced by ΔV_{GS}.

$$\mu = \frac{\Delta I_{DS}}{C_{ox}\frac{W}{L}V_{DS}\Delta V_{GS}} \quad (1)$$

Using the FET parameters given above, the hole and electron mobilities were extracted to be $\mu_h = 3735$ cm^2/Vs and $\mu_e = 795$ cm^2/Vs, respectively. The maximum drive current (I_{DS}/W) at $V_{DS} = 1$ V is 1.7 mA/μm. The mobilities and the drive current are among the highest values reported.[4,5,16] The hole mobility in our devices is about five times higher than the electron mobility, which is consistent with previous work in graphene FETs fabricated by exfoliation and epitaxial growth.[4,5] This asymmetry in carrier mobilities, contradicting the prediction based on the symmetry of ideal graphene's conduction and valance bands, is attributed to the extrinsic doping during the preparation or handling of materials.[4,5]

For a fixing layer that uses O_2 plasma treatment, we found that the plasma treatment can increase the bonding strength to a graphene significantly but degrade the carrier transport properties. For example, a graphene transistor fabricated using O_2 plasma treatment bonding ($t_{ox} = 50$ nm, $W = 1.2$ μm, $L = 11$ μm, and $d = 1.5$ nm) has $I-V$ characteristics shown in Figure 5. The I−V shows only the dominating hole conduction but no electron conduction, and a hole mobility of 991 cm^2/Vs, which is about 3 times smaller than that for graphene FETs bonded to a substrate without O_2 plasma treatment. One of possible reasons for such mobility reduction and the loss of the electron conduction could be attributed to the dangling bonds generated by the plasma, which increases the bonding strength but also increases the density of surface charge traps, which can shift the transition point and degrades the mobility.

Here, the graphene FETs exhibit a relatively weak gate modulation (ON−OFF current ratio) in comparison with typical silicon-based FETs. This is because of the fact that graphenes are a two-dimensional zero-band gap semiconductor (or a semimetal) rather than a semiconductor with a gap. Its screening length is very thin (~0.5 nm, which is less than two graphene monolayers). These two reasons make graphene transistors having a significant OFF current.[1,17,18] Therefore to reduce the OFF current, one needs to create a band gap in graphene and use the monolayer. Theory indicates

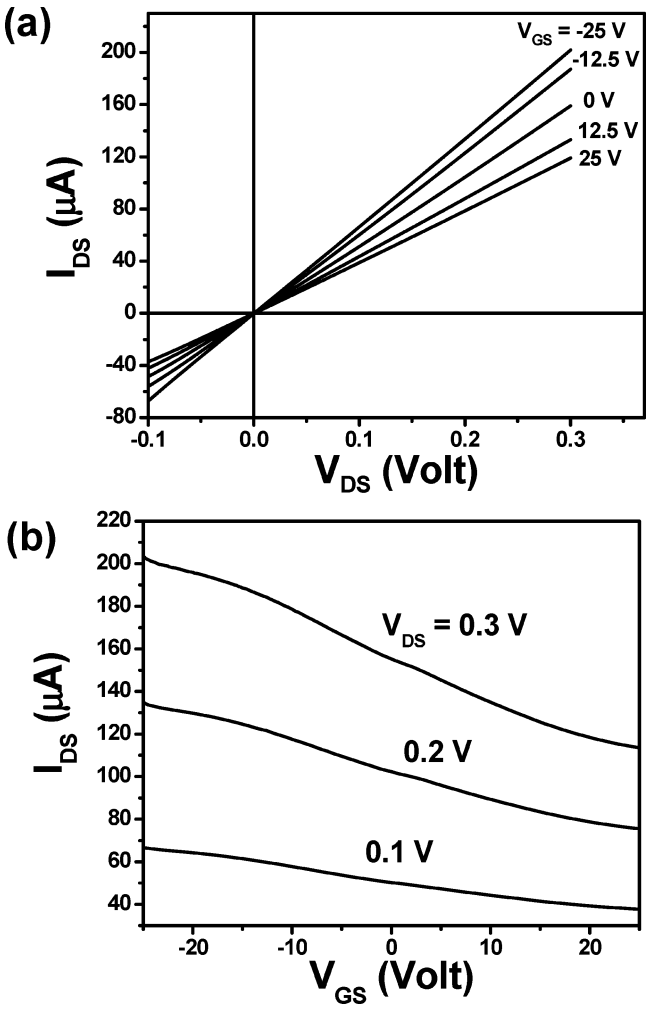

Figure 5. The characteristics of a graphene FET fabricated through the O_2 plasma-assisted DCT process: (a) I_{DS} vs V_{DS} for $V_{GS} = -25, -12.5, 0, 12.5, 25$ V (back gate field from −5 to 5 MV/cm); (b) I_{DS} vs V_{GS} for $V_{DS} = 0.1, 0.2, 0.3$ V. The transistor shows only the hole conduction, and the hole mobility is about 3 times smaller than that shown in Figure 4.

graphene could have a band gap by using the edge states in a narrow width graphene strip.[17,19]

In summary, we have demonstrated a method that can cut and transfer/print graphenes into the desired device active areas on a large substrate (i.e., graphene-on-demand) and have achieved working FETs with good transport properties. Such an approach might have applications to build graphene integrated circuits on large wafers.

References

(1) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. *Science* **2004**, *306* (5696), 666−669.

(2) Artukovic, E.; Kaempgen, M.; Hecht, D. S.; Roth, S.; Gruner, G. *Nano Lett.* **2005**, *5* (4), 757−760.

(3) Natori, K.; Kimura, Y.; Shimizu, T. *J. Appl. Phys.* **2005**, *97*, (3).

(4) Lemme, M. C.; Echtermeyer, T. J.; Baus, M.; Kurz, H. *IEEE Electron Device Lett.* **2007**, *28* (4), 282−284.

(5) Gu, G.; Nie, S.; Feenstra, R. M.; Devaty, R. P.; Choyke, W. J.; Chan, W. K.; Kane, M. G. *Appl. Phys. Lett.* **2007**, *90*, (25).

(6) Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. *Appl. Phys. Lett.* **1995**, *67* (21), 3114−3116.

(7) Chou, S. Y.; Krauss, P. R. *Microelectron. Eng.* **1997**, *35* (1−4), 237−240.

(8) Gao, H.; Tan, H.; Zhang, W.; Morton, K.; Chou, S. Y. *Nano Lett.* 2006.
(9) Kim, C.; Burrows, P. E.; Forrest, S. R. *Science* **2000**, *288* (5467), 831−833.
(10) Kong, Y. P.; Tan, L.; Pang, S. W.; Yee, A. F. *J. Vac. Sci. Technol., A* **2004**, *22* (4), 1873−1878.
(11) Kim, C.; Shtein, M.; Forrest, S. R. *Appl. Phys. Lett.* **2002**, *80* (21), 4051−4053.
(12) Loo, Y. L.; Willett, R. L.; Baldwin, K. W.; Rogers, J. A. *J. Am. Chem. Soc.* **2002**, *124* (26), 7654−7655.
(13) Pasquariello, D.; Hjort, K. *IEEE J. Sel. Top. Quantum Electron.* **2002**, *8* (1), 118−131.
(14) Weinert, A.; Amirfeiz, P.; Bengtsson, S. *Sens. Actuators, A* **2001**, *92* (1−3), 214−222.
(15) Li, N. H.; Wu, W.; Chou, S. Y. *Nano Lett.* **2006**, *6* (11), 2626−2629.
(16) Inokawa, H.; Nagase, M.; Hirono, S.; Goto, T.; Yamaguchi, H.; Torimitsu, K. *Jpn. J. Appl. Phys., Part 1* **2007**, *46* (4B), 2615−2617.
(17) Novoselov, K. S.; Geim, A. K. *Nat. Mater.* **2006**, *6* (3) 183−191.
(18) Miyazaki, T.; Kanayama, T. *Appl. Phys. Lett.* **2007**, *91* (8), 082107.
(19) Son, Y. W.; Cohen, M. L.; Louie, S. G. *Phys. Rev. Lett.* **2006**, *97* (8), 216803.

NL072566S